FUDAN MICROELECTRONICS

复旦微电子

FM11RF005M
512Bits EEPROM Contactless Smart Card IC

Functional Specification

May. 2008

Content

1. Features

- **Contactless Communications RF Interface**
  - Contactless transmission of data and supply (no battery needed)
  - Operating distance: up to 100mm (depending on antenna geometry)
  - Operating frequency: 13.56MHz
  - High data transmission rate: 106Kbit/s
  - Half duplex communication protocol using handshake
  - Modulation and encoding comply with ISO/IEC 14443-A protocol
  - Answer to request: comply with ISO/IEC14443-A protocol
  - Encryption algorithm compatible with M1
  - Typical transaction time: ≤ 35ms
  - Collision transaction: RWD doesn't transact all of the two or more cards that appear at the antenna field simultaneity.
- **EEPROM**
  - 512 bits EEPROM memory.
  - Organized in 16 blocks of 4 bytes each
  - Flexible data structure
- **High Security**
  - 32 bits serial number of chip
  - High security level data communication (mutual three pass authentication、Access right control)
  - Security levels control
- **Low-cost**
- **High Reliability**
  - Endurance: >100,000 cycle
  - Data Retention: >10 Years

2. Product Overview

2.1. Instruction

The FM11RF005M is the contactless smart card IC according to ISO14443-A developed by Shanghai FM Co., This device has 512 bits EEPROM organization. The maximum communication range between the reader antenna and contactless card is approximately 10cm. Data is exchanged half duplex at a 106-kbit/s rate.

Depending on the encryption control unit and communication logic circuitry FM11RF005M provides advanced security level and logical transaction function. The FM11RF005M is wildly used in the low-cost field of city public transport、variously charging payment card、data acquisition systems and comparable application.

The FM11RF005M contains three components: the FM11RF005M chip、antenna and the card base with PVC (or PET) material. No battery is needed. When the chip is positioned in proximity of the coupling device antenna, the high speed RF communication interface allows transmitting data with 106 Kbit/s.

2.2. Block Diagram

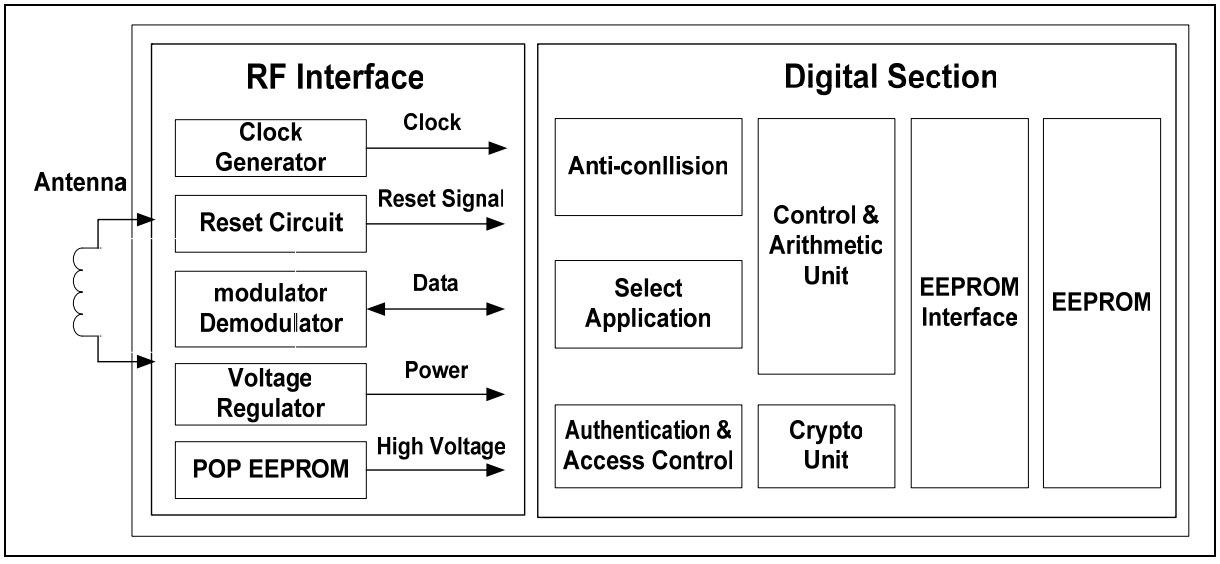

Figure 2-1 FM11RF005M Block Diagram

3. Command Set

3.1. Command Description

REQALL/REQA: establishes the communication between card and RWD, the REQALL/REQA command has to be passed before implementing the further commands.

Read: read one block.

Write: write one block at twice, first send a WRITE command and the address to card, after acknowledges it is right the card will answer a response, and then transmit the data waiting to be written.

Authentication: Authentication between the card and RWD adopts the mutual three pass authentication.

3.2. Command Format

The format of chip's communication command is shown as figure 3-2:

Byte No. / command	0	1	2	3	4	5	6	7	Return value (correct)	Return value (wrong)
REQALL/ REQA	52H/ 26H	unused	unused	unused	unused	unused	unused	unused	CID	Not ACK
READ	30H	ADDR	CRC	CRC	unused	unused	unused	unused	Read out data+CRC	0001 (communication error)
WRITE	0A0H	ADDR	CRC	CRC	unused	unused	unused	unused	1010	
	DATA	DATA	DATA	DATA	CRC	CRC	unused	unused	1010	0000 (other error)
AUTH	60H	ADDR	CRC	CRC	unused	unused	unused	unused	Rb	Not ACK
	Ra0	Ra1	Ra2	Ra3	Ra4	Ra5	Ra6	Ra7	Rb'	Not ACK

Table 3-1 FM11RF005M Command Format

Note:

1. All of above are the commands that RWD send to card.
2. Maintain two commands of 'REQA' and 'REQALL' for be accordance with shanghai public traffic card.
3. "Unused "denotes not send this byte.
4. CRC in the Table 3-1 adopts the polynomial of CRC-CCITT standard:
   $G(X) = X^{16}+X^{12}+X^{5}+1$

5. In communication there is a parity bit after each byte, but parity bits don't be implemented the CRC.
6. There is no CRC after the CID if the REQA response
7. If the authentication is returned correctly, no CRC.
8. The error return value is 4 bits.

Error Reason	Error Return Value
CRC error	01
Parity bits error	01
Mistaken command	01
No right	not acknowledge
Authentication defeat	not acknowledge

Table 3-2 FM11RF005M Error Reason of the Return Value

4. Transaction Sequence

Transaction sequence is shown below:

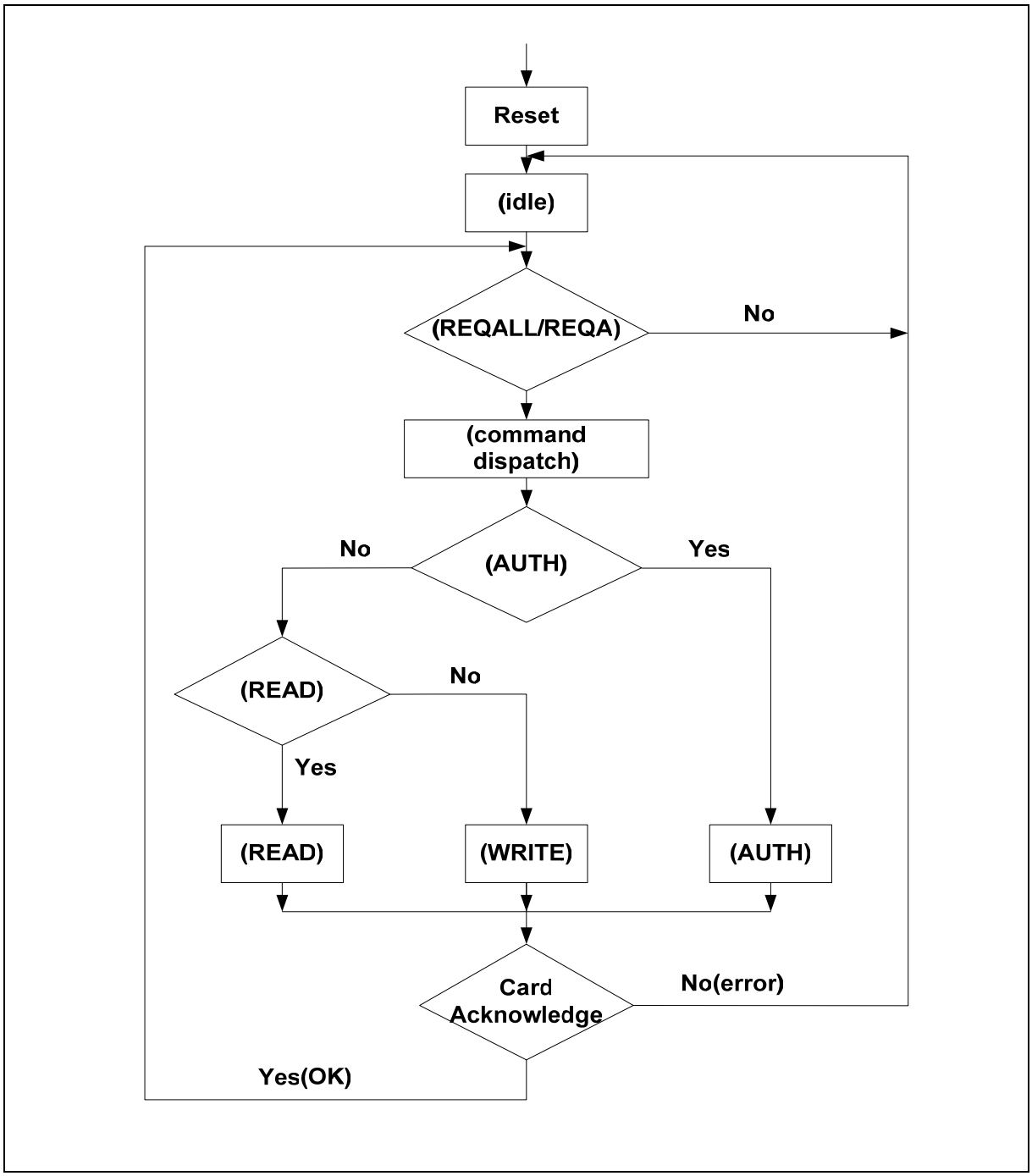

Figure 4-1 FM11RF005M Transaction Sequence

5. Memory Organization

5.1. Blocks Assignation and Access Right

The general purpose memory of FM11RF005M is divided into 16 blocks; each block consists of 4 bytes of 8 bits each. Read/Write operation acts on blocks. FM11RF005M's access right is shown as Table 5-1:

Block Number	Never authenticated		Have authenticated	
	Read	write	Read	write
0~1	Yes	No	Yes	No
2~7	Yes	No	Yes	Yes
8~15	No	No	Yes	Yes

Table 5-1 FM11RF005M Access Right of EEPROM

Chip code consists of Customers ID(CID)、Manufacturers ID(MID) and the serial number of chip(SN).

Customers ID adopt the code defined by administrative organizations of standardization; Manufacturers ID adopt the code defined by administrative organizations of IC card registration; the serial number of chip is the ID generated during the procession of manufacture.

The code of every chip is unique and write-protected after having been programmed by the IC manufacturer after production, user can't change those. The chip code holds two data blocks (Block0、Block1). The byte 0 and byte 1 of block 0 are used to store the CID. The byte2 and byte3 of block 0 is used to store the MID. The SN is stored in the block1.

The data storage format of chip code is defined complies with show below:

Byte / Block	0	1	2	3
0	Customer ID（CID）		Manufacturer ID（MID）	
1	Chip serial number			

Table 5-2 FM11RF005M Data Storage Format of Chip Code

Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
1.0	Oct. 2007	11		Initial Release.
1.1	May. 2008	11	Sales and service	Updated the address of HK office.

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